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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,876	03/10/2004	Anthony Dip	TPS-007	5070

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WOOD, HERRON & EVANS, LLP (TOKYO ELECTRON)
2700 CAREW TOWER
441 VINE STREET
CINCINNATI, OH 45202

EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	**PAPER NUMBER**
2811	

NOTIFICATION DATE	DELIVERY MODE
11/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

dgoodman@whepatent.com
usptodock@whepatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/797,876	DIP ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,13-21 and 26* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,13-20 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 and 10-20 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, 20 and 26 recite the limitation "an unreacted portion of the SiGe surface layer" in lines 6-7, line 12, and line 6 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 13-16, 18-20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Effects of low-temperature water vapor annealing of strained SiG surface-channel pMOSFETs with high-K dielectric to Westlinder et al. (Westlinder) as cited in IDS filed 08/11/2005 in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland).

Regarding claim 1, Westlinder discloses a method of forming a semiconductor device, the method comprising:

providing a substrate (Fig 1 "n-well" area);

forming a SiGe surface layer (Fig 1 "10 nm SiGe) on the substrate;

depositing a high-k dielectric layer (Fig 1 "High-k") onto the SiGe surface layer; and

forming an oxide layer (interfacial oxide not shown in Figure but disclosed; page 525 col 1 paragraph 3 last lines 10-11; page 526 col 2 line 1) between the high-k dielectric layer and an unreacted portion of the SiGe surface layer, the oxide layer being formed during one or both of said depositing and an annealing process after said depositing (C-V after depositing and annealing of high-k dielctric resulted in the finding of the oxide layer; page 526 col 2 line 1)

forming an electrode layer (Fig 1 "TiN gate") on the high-k dielectric layer.

Westlinder fails to explicitly disclose the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24)
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Westlinder to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Regarding claim 2, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder fails to disclose the substrate provided with

an initial oxide layer. Hareland also discloses the substrate provided with an initial oxide layer (Figures 5A-5E, element 506, col 9 lines 9-12) prior to forming the SiGe (508/520) surface layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Westlinger to have an initial oxide as in Hareland in order to provide for improved device isolation.

Regarding claim 3, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder also includes forming the SiGe surface layer by performing thermal chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer deposition, or sputtering (chemical vapor deposition, page 525 col 2 section 2 line 5).

Regarding claim 13, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder also discloses the SiGe surface layer is less than about 1000 angstroms thick (10 nm, see Figure 1, which is 100 angstroms thick).

Regarding claim 14, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder also discloses the SiGe surface layer is between about 10 - 300 angstroms thick (10 nm, see Figure 1, which is 100 angstroms thick).

Regarding claim 15, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder also discloses the high-k dielectric layer comprises at least one of HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, TiO_2, Ta_2O_5, Al_2O_3, or SiN (Al_2O_3 page 525 col 2 section 2 lines 8-9).

Regarding claim 16, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder also discloses the high-k dielectric layer is between about 5 – 60 angstroms thick (30 Å, page 525 col 2 section 2 lines 20-21; 28 Å, page 526 col 1 last 5 lines).

Regarding claim 18, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder fails to disclose etching the elecltoryde and high-k dielectric layer. Hareland also discloses etching the electrode layer and the high-k dielectric layer (col 11, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Westlinder to etch the electrode layer and high-k dielectric layer in order to form devices on the substrate.

Regarding claim 19, Westlinder in view of Hareland discloses the method according to claim 1 as above and Westlinder further discloses the oxide layer formed during the annealing process by exposing the substrate to an oxygen containing gas (exposed to water vapor anneal, page 526 col 1 paragraph 3, and oxygen is present in H_2O).

Regarding claim 20, Westlinder discloses a method of forming a semiconductor device, the method comprising:

providing a substrate (Fig 1 "n-well" area);

forming a SiGe surface layer (Fig 1 "10 nm SiGe) on the substrate;

depositing a high-k dielectric layer (Fig 1 "High-k") onto the SiGe surface layer;

annealing the substrate having the SiGe and high-k dielectric thereon (page 526 col 1 paragraphs 2-3); and

forming an electrode layer (Fig 1 "TiN gate") on the high-K dielectric layer.

wherein at least one of the depositing and annealing comprising exposing the substrate to an oxygen-containing gas (exposed to water vapor anneal, page 526 col 1 paragraph 3, and oxygen is present in H_2O) to form an oxide layer between the dielectric layer and an unreacted portion of the SiGe surface layer (interfacial oxide not shown in Figure but disclosed C-V after depositing and annealing of high-k dielectric resulted in the finding of the oxide layer; page 525 col 1 paragraph 3 last lines 10-11; page 526 col 2 line 1).

Westlinder fails to explicitly disclose the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24)
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Westlinder to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Regarding claim 26, Westlinder discloses a method of forming a semiconductor device, the method comprising:

providing a substrate (Fig 1 "n-well" area);

forming a SiGe surface layer (Fig 1 "10 nm SiGe) on the substrate;

depositing a high-k dielectric layer (Fig 1 "High-k") onto the SiGe surface layer;

forming an oxide layer (interfacial oxide not shown in Figure but disclosed; page 525 col 1 paragraph 3 last lines 10-11; page 526 col 2 line 1) between the high-k

dielectric layer and an unreacted portion of the SiGe surface layer, the oxide layer being formed during one or both of said depositing and an annealing process after said depositing (C-V after depositing and annealing of high-k dielctric resulted in the finding of the oxide layer; page 526 col 2 line 1); and

forming an electrode layer (Fig 1 "TiN gate") on the high-K dielectric layer. Westlinder fails to explicitly disclose the substrate as a single crystal silicon or polycrystalline silicon and also fails to disclose the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses a substrate of single crystal silicon or polycrystalline silicon (col 3 lines 34-67) and a SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Westlinder to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Effects of low-temperature water vapor annealing of strained SiG surface-channel pMOSFETs with high-K dielectric to Westlinder et al. (Westlinder) as cited in IDS filed 08/11/2005 in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and in view of EP 0684 650 B1 to Hiroshi et al. (Hiroshi) as cited in IDS filed 03/10/2004.

Regarding claims 4-5, Westlinder in view of Hareland discloses the method according to claim 1 as above. Westlinder in view of Hareland fails to disclose forming

the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$. Hiroshi includes forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$ (GeH_4, paragraph [0046]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Westlinder to have the form the SiGe surface layer as in Hiroshi to provide a high quality SiGe layer.

Regarding claim 6, Westlinder as modified discloses the method according to claim 4 as above. Westlinder discloses annealing the substrate either during said exposing, after said exposing, or both during and after said exposing (page 526 col 1 paragraphs 2-3).

Regarding claims 7-8, Westlinder in view of Hareland discloses the method according to claim 4 as above. Westlinder in view of Hareland fails to disclose the process gas comprising a Si-containing gas comprising at least one of SiH_4, Si_2H_6, or SiH_2Cl_2. Hiroshi includes the Si-containing gas comprising at least one of SiH_4, Si_2H_6, or SiH_2Cl_2 (Si_2H_6, paragraph [0046]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Westlinder to have the form the SiGe surface layer as in Hiroshi to provide a high quality SiGe layer.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Effects of low-temperature water vapor annealing of strained SiG surface-channel pMOSFETs with high-K dielectric to Westlinder et al. (Westlinder) as cited in IDS filed

08/11/2005 in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and U.S. Pub. No. 2003/0218189 to Christiansen et al. (Christiansen).

Regarding claims 10 and 11, Westlinder in view of Hareland discloses the method according to claim 1 above. Westlinder fails to disclose the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and also fails to disclose the SiGe surface layer comprising a graded Ge content.

Christiansen discloses a plurality of SiGe sublayers (Figure 8 layers 45, 42, 25, and 35) each with different Ge content (paragraph 82, last 3 lines) and the SiGe surface layer with a graded Ge content (Figure 9 layers 46, 37, 37 and 43, paragraph 38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Westlinder to have the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and the SiGe surface layer comprising a graded Ge content as in Christiansen in order to reduce defects normally present in a single SiGe layer (Christiansen, paragraph 15).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Effects of low-temperature water vapor annealing of strained SiG surface-channel pMOSFETs with high-K dielectric to Westlinder et al. (Westlinder) as cited in IDS filed 08/11/2005 in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and U.S. Pat. No. 5,259,881 to Edwards et al. (Edwards).

Regarding claim 17, Westlinder in view of Hareland discloses the method according to claim 1 as above with an Si substrate. Westlinder in view of Hareland fails

to disclose introducing the substrate into a process chamber of one of a single wafer processing system and a process chamber of a batch-type processing system. Edwards teaches introducing a substrate into a process chamber of a batch-type processing system (col 3 lines 6-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Westlinder to include introducing the Si substrate into a process chamber of a batch-type processing system in order to maximize the add to the speed and flexibility of the substrate processing (Edwards, lines 14-17).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/12/2007
CAM

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800